

ARYAN CHAHARDOVALEE

Electrical engineer focused on RF systems, flight test, and hardware validation.

San Francisco Bay Area | +1 (415) 800-3435 | arianchahardovalee@gmail.com | linkedin.com/in/aryan-chahardovalee | aryanch.com | GitHub: aryanxoxo

PROFESSIONAL SUMMARY

Electrical engineer with hands-on experience across autonomous aircraft flight test, RF and wireless systems, embedded hardware, PCB/debug workflows, FPGA design, satellite communications, maritime EMC/EMI, and engineering documentation. Comfortable moving between bench work, field operations, simulation, test automation, and clear written evidence. Portfolio includes repo-backed and media-backed projects in UAS communications, SDR receivers, CubeSat radio links, FPGA systems, microcontroller instrumentation, MRI RF pulse simulation, and photonics.

TECHNICAL SKILLS

Hardware Validation & Test: Flight-test support, preflight/recovery checks, DVT-style test plans, bench debug, field diagnostics, failure isolation, test reports, procedure discipline

RF / Wireless / Telecom: 433/437 MHz CubeSat links, SDR, ADS-B, AIS, SatNOGS-style ground station, link budgets, BER modeling, antennas, VNA/spectrum analyzer/oscilloscope workflows

Embedded / Robotics / UAS: Drone sensor integration, camera/IMU/LiDAR/WLAN systems, STM32, EFM8, AT89LP51RC2, C/C++, Python, serial interfaces, GPS/Wi-Fi/RF links

FPGA / Digital Systems: Verilog, VHDL, DE1-SoC, Nios II/Qsys, DDS/modulation, RC4 FSMs, RISC datapath, VGA/PS2, SPI/ADC/DAC interfaces

PCB / Electrical Design: KiCad/Altium exposure, RF PCB review, SMA launches, matching networks, grounding/return paths, soldering/debugging, power/load analysis

Software / Analysis: Python, MATLAB, Streamlit, data visualization, signal processing, notebooks, Git/GitHub, Linux setup scripts, automation and documentation

EXPERIENCE

Flight Test Operator / Engineering Flight Test Operations | Zipline International, Half Moon Bay, CA (Nov 2024 - Jun 2026)

- Supported autonomous aircraft flight-test execution across preflight, launch, recovery, readiness checks, hardware/software checks, and post-test documentation in outdoor test environments.
- Troubleshoot UAV communication and electromechanical issues during live operations, escalating clear observations to engineering and operations teams for resolution.
- Maintained FAA-certification-style procedural discipline where safety, aircraft state, RF link reliability, timing, and operator handoffs all had to stay controlled.
- Translated field observations into practical engineering feedback on aircraft readiness, communication reliability, and operational repeatability.

Hardware / AI Integration Team Member | Huawei Canada Capstone Project, Burnaby, BC (Sep 2022 - Apr 2023)

- Built and tested an autonomous drone prototype integrating camera, IMU, LiDAR, WLAN, sensor-board power, and real-time perception inputs.
- Configured WLAN links between drone, sensors, and AI board, improving response speed by roughly 250 percent compared with the previous prototype baseline.
- Recalibrated camera and IMU systems, replaced damaged propellers after test failures, debugged integration issues, and supported rapid hardware/software prototype loops.
- Provisioned secondary power for sensor electronics, reducing primary battery load and extending flight time by roughly 7 minutes / 60 percent in project testing.

RF & Wireless Systems Engineer | UBC ORBIT Satellite Design Team, Vancouver, BC (Jan 2019 - Apr 2023)

- Developed and tested RF communication and antenna-deployer PCB concepts for CubeSat hardware, including 433 MHz downlink analysis and deployment reliability concerns.
- Integrated OpenLST SDR / CC1110-style radio hardware and improved link behavior through radio-system iteration, BER reasoning, and link-budget analysis.
- Troubleshoot antenna deployment failure modes through PCB iteration and bypass-feature design, strengthening hardware reliability under mission constraints.
- Worked across communications, payload, power, and controls interfaces; helped junior members understand subsystem integration and satellite control sequences.

Electronics Engineering Intern | Seaspan ULC / Vancouver Shipyards, North Vancouver, BC (Sep 2021 - May 2022)

- Drafted design reports, test agendas, block diagrams, and trade studies for shipboard communication subsystems including Wi-Fi, VHF, HF, UHF, NAVTEX, GMDSS, and SATCOM.
- Executed RF characterization, OTA antenna testing, and EMC/EMI studies using FEKO Altair, HFSS/CST-style workflows, and HPC simulation resources.

- Built Python analysis/test automation that improved test efficiency by roughly 30 percent and helped increase simulation throughput by more than 300 percent.
- Supported modernization decisions by identifying obsolete components, evaluating vendor feedback, and recommending reliability improvements for marine systems.

Undergraduate Researcher | UBC SiEPIC Photonics Lab, Vancouver, BC (2023)

- Designed and tested high-Q Fabry-Perot resonators and DFB laser structures; automated optical characterization and visualization workflows in Python.
- Operated lab instrumentation and built repeatable measurement habits relevant to prototype validation, calibration, and technical reporting.

Exclusive Partner Program Member | TELUS, Vancouver, BC (2024)

- Worked in a technical customer-facing role that strengthened requirements translation, practical device/service troubleshooting, and concise explanation of technical options.

SELECTED PROJECT EVIDENCE

WLAN for Huawei Drone - UAS communications / WLAN / hardware integration

- Designed and characterized a drone WLAN command-and-control path connecting drone, sensors, AI board, and Internet-connected Wi-Fi hardware.
- Documented architecture, start/stop strategy, test behavior, and demo evidence for sponsor review.
- Portfolio evidence: demo video, diagrams, and Capstone13 GitHub repository.

UAV Telemetry Link Monitor - ESP32 / LoRa / Python dashboard / Parrot Anafi payload

- Built a repo-backed telemetry monitor using an independent ESP32 + LoRa payload on a Parrot Anafi and a ground-station ESP32 receiver.
- Dashboard reads serial JSON when hardware is connected and shows RSSI, SNR, packet loss, latency, antenna geometry, range/bearing, and CSV logs.

433 MHz CubeSat Radio Link - RF link budget / BER / CubeSat communications

- Built a public proof trail with link-budget model, BER model, example data, plots, and notebook-style engineering analysis.
- Shows how assumptions, range, EIRP, path loss, noise figure, Eb/N0, and link margin affect CubeSat radio feasibility.

SatNOGS Ground Station - Linux / SDR / satellite communications

- Created Linux setup scripts and a runbook for an SDR-based amateur satellite ground-station workflow.
- Covers SDR device setup, pass planning, telemetry capture, and local run instructions without requiring a public online dashboard.

SDR ADS-B Receiver - Python / SDR / aviation RF

- Built a repo-backed ADS-B receiver lab showing Mode S / ADS-B decode flow, local execution, and receiver proof trail.
- Useful evidence for RF, aviation, signal decoding, and Linux/Python field-tooling roles.

AIS Marine Receiver - Python / NMEA / maritime RF

- Built a Python AIS receiver with NMEA vessel parsing and local map/dashboard workflow for live vessel traffic experiments.
- Connects maritime communication experience to SDR and software tooling.

MRI Slice-Selective RF Pulse Designer - Python / Streamlit / MRI physics

- Created an interactive RF pulse simulator with Bloch-equation-style spin excitation, slice-selection controls, presets, and waveform/FFT plots.
- Demonstrates engineering communication, physics modeling, and browser-accessible analysis tooling.

Custom 2.4 GHz RF Front-End PCB - KiCad / RF layout / SMA launch

- Designed a 2.4 GHz RF front-end PCB preview with 50 ohm microstrip, SMA connectors, matching network, RF amplifier, decoupling, and via-fence/grounding concepts.
- Shows RF layout thinking around return paths, signal flow, component placement, and reviewable board evidence.

OFDM Modem Simulation - MATLAB / DSP / wireless communications

- Built an OFDM simulation preview with time-domain waveform, 64-subcarrier data/pilot allocation, QPSK constellation, MMSE equalizer, Rayleigh channel behavior, and BER curves.
- Evidence aligns with telecom, RF systems, and signal-processing roles.

AI Lab Bench Assistant - Python / SCPI / PyVISA / test automation

- Built a simulated lab-bench assistant for instrument-style workflows, report generation, and structured test capture.
- Relevant to validation automation and bench-test documentation roles.

SCADA Robot Arm - SCADA / PID / controls / mechanical simulation

- Converted an electrical report and simulation evidence into portfolio proof, including project picture and demo video.
- Shows controls thinking, report writing, and engineering presentation of a mechatronics system.

Fabry-Perot Cavity Resonators - Silicon photonics / SiEPIC / Lumerical-style analysis

- Designed photonic resonator structures and captured evidence through reports, layout imagery, and lab/simulation workflow.
- Connects optics, device design, and Python-based characterization.

FPGA Signal Processing with Nios II, DDS, and Modulation Techniques - Verilog / VHDL / Nios II / Qsys

- Organized a clean public source archive with HDL, Qsys files, C software, DDS/LFSR modulation logic, and ModelSim evidence.
- Implemented ASK/BPSK/FSK-style signal generation and VGA oscilloscope-style visualization on FPGA hardware.

RC4 Decryption Circuit with Modular FSM Design - Verilog / SystemVerilog / FPGA cryptography

- Built a clean source archive for an RC4 decryption datapath using modular FSMs, RAM/ROM message memory, key-search logic, and testbenches.
- Shows finite-state-machine design, memory interfaces, hardware debugging, and verification structure.

Simple RISC Machine using Verilog and the DE1-SoC - Verilog / CPU datapath / ALU / register file

- Organized CPU, datapath, ALU, shifter, register file, top-level wrapper, Quartus files, and ModelSim project evidence into a dedicated repo.
- Relevant to digital design, computer architecture, and FPGA validation roles.

FPGA-Powered iPod - Verilog / PicoBlaze / flash memory / audio path

- Built a clean public archive of the FPGA audio-player design including keyboard control, LCD/scope display logic, PicoBlaze support files, and ModelSim benches.
- Shows practical state-machine integration across user input, memory, audio timing, and hardware display paths.

Embedded Instrumentation Projects - STM32 / EFM8 / 8051 / LCD / serial interfaces

- Metal detector using STM32, capacitance meter using EFM8, alarm clock using AT89LP51RC2, and autonomous reflow oven control project.
- Evidence includes bench photos, local videos, firmware-oriented descriptions, LCD readouts, and measurement/control behavior.

EDUCATION AND CREDENTIALS

Bachelor of Applied Science, Electrical Engineering - University of British Columbia, 2018 - 2023

Credentials: FAA Part 107 Remote Pilot Certificate; FCC Restricted Radiotelephone Operator Permit (RR); ROC-A aeronautical radio qualification; Amateur Radio License VA7AYO; Google Cybersecurity Certificate; EGBC Engineer-in-Training credential shown on homepage for Canadian context.

Aviation: Private pilot training with 70+ hours in Cessna 152; BCIT Airline and Flight Operations coursework completed for two terms in 2024.

Clearance / compliance exposure: Reliability and Controlled Goods clearance experience through Seaspan / Canadian shipbuilding environment.

TARGET ROLES

Hardware validation engineer; electrical engineer; RF systems engineer; flight test instrumentation engineer; UAS test engineer; embedded hardware engineer; test automation engineer; FPGA validation / digital systems engineer; robotics hardware technician.

Portfolio: aryanch.com - selected projects include source archives, reports, screenshots, videos, runbooks, hardware photos, and local-dashboard workflows.